What is claimed is:

1. A semiconductor which consists of a compound single crystal and comprises a region (referred to as "high-defect-density region", hereinafter) having a planar defect density of $1 \times 10^7/cm^2$ or more and a region (referred to as "low-defect-density region", hereinafter) having a planar defect density of $1/cm^2$ or less.

2. The semiconductor according to claim 1, wherein the high-density defect region has an electron concentration of 10 times or more of that of the low-defect-density region at room temperature.

3. The semiconductor according to claim 1 or 2, wherein the semiconductor has a plate shape having at least one pair of opposite surfaces that are roughly parallel, on one surface (referred to as "high-defect-density surface", hereinafter) of which, the high-defect-density region is exposed, and, on the other surface (referred to as "low-defect-density surface", hereinafter) of which, the low-defect-density region is exposed.

4. The semiconductor according to claim 1, wherein the planar defect is at least one of anti-phase boundary, stacking fault, and small-angle grain boundary.

5. The semiconductor according to claim 1, wherein the compound single crystal is a group IV-IV compound single crystal, a group III-V compound single crystal, or a group II-VI compound single crystal.

6. The semiconductor according to claim 1, wherein the compound single crystal is a cubic type crystal.

7. The semiconductor according to claim 1, wherein the semiconductor has a transition region, between the high-defect-density region and the low-defect-density region, having a thickness of 5 μ m or less and a gradient of defect density of $4 \times 10^9/cm^3$ or more.

8. A semiconductor substrate, wherein a semiconductor is provided on a substrate and said semiconductor consists of a compound single crystal and comprises a region (referred to as "high-defect-density region", hereinafter) having a planar defect density of $1 \times 10^7/cm^2$ or more and a region (referred to as "low-defect-density region", hereinafter) having a planar defect density of $1/cm^2$ or less.

9. The semiconductor substrate according to claim 8, wherein the high-density defect region has an electron concentration of 10 times or more of that of the low-defect-density region at room temperature.

10. The semiconductor substrate according to claim 8, wherein the semiconductor has a plate shape having at least one pair of opposite surfaces that are roughly parallel, on one surface (referred to as "high-defect-density surface", hereinafter) of which, the high-defect-density region is exposed, and, on the other surface (referred to as "low-defect-density surface", hereinafter) of which, the low-defect-density region is exposed.

11. The semiconductor substrate according to claim 8, wherein the planar defect is at least one of anti-phase boundary, stacking fault, and small-angle grain boundary.

12. The semiconductor substrate according to claim 8, wherein the compound single crystal is a group IV-IV compound single crystal, a group III-V compound single crystal, or a group II-VI compound single crystal.

13. The semiconductor substrate according to claim 8, wherein the compound single crystal is a cubic type crystal.

14. The semiconductor substrate according to claim 8, wherein the semiconductor has a transition region, between the high-defect-density region and the low-defect-density region, having a thickness of 5 μm or less and a gradient of defect density of $4 \times 10^9/cm^3$ or more.

15. The semiconductor substrate according to claim 8, wherein the semiconductor comprises a high-defect-density region and a low-defect-density region in this order on a substrate.

16. A method of manufacturing the semiconductor according to claim 1 or the semiconductor substrate according to claim 8, in which a compound single crystal is grown on a substrate using liquid phase or vapor phase, and the method comprises the steps of;

growing a compound single crystal having a planar defect at a density of $1 \times 10^7/cm^2$ or more on the surface of the growth substrate(referred to as "step (A)", hereinafter), and

growing a compound single crystal in an orientation differing from an orientation of propagation of the planar defect exposed on the surface of the compound single crystal grown in the step (A) to form a compound single crystal layer having a planar defect density of $1/cm^2$ or less (referred to as "step (B)", hereinafter).

17. The method according to claim 16, wherein the step (A) is carried out by generating a planar defect at a density of 1 x $10^7/cm^2$ or more on the surface of the substrate as well as constantly exposing the planar defect on the surface to propagate the structure of the planar defect.

18. The method according to claim 16, wherein, following forming the compound single crystal layer having a planar defect density of $1/cm^2$ or less, the growth substrate is removed to obtain the semiconductor according to claim 1.

19. A semiconductor device comprising a semiconductor, an electrode having at least one ohmic contact, and an electrode having at least one non-ohmic contact, wherein the semiconductor consists of a compound single crystal and comprises a region (referred to as "high-defect-density region", hereinafter) having a planar defect density of 1 x $10^7/cm^2$ or more and a region (referred to as "low-defect-density region", hereinafter) having a planar defect density of $1/cm^2$ or less, and the ohmic contact is formed in the high-density defect region of the semiconductor and the non-ohmic contact is formed in the low-density defect region of the semiconductor.

20. The semiconductor device according to claim 19, wherein the high-density defect region has an electron concentration of 10 times or more of that of the low-defect-density region at room temperature.

21. The semiconductor device according to claim 19, wherein the semiconductor has a plate shape having at least one pair of opposite surfaces that are roughly parallel, on one surface (referred to as "high-

defect-density surface", hereinafter) of which, the high-defect-density region is exposed, and, on the other surface (referred to as "low-defect-density surface", hereinafter) of which, the low-defect-density region is exposed.

22. The semiconductor device according to claim 19, wherein the planar defect is at least one of anti-phase boundary, stacking fault, and small-angle grain boundary.

23. The semiconductor device according to claim 19, wherein the compound single crystal is a group IV-IV compound single crystal, a group III-V compound single crystal, or a group II-VI compound single crystal.

24. The semiconductor device according to claim 19, wherein the compound single crystal is a cubic type crystal.

25. The semiconductor device according to claim 19, wherein the semiconductor has a transition region, between the high-defect-density region and the low-defect-density region, having a thickness of 5 μ m or less and a gradient of defect density of $4 \times 10^9/cm^3$ or more.